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Analytical Investigations on carrier recovery for a 16-QAM Receiver used in software defined radio

Mansi Kapahi, Amandeep Singh Sappal

Abstract: In this paper analytical investigation has been done on the closed-loop carrier recovery scheme for a 16-QAM receiver. Additional filter called randomwalk filter has also been used to reduce symbol clock jitter, particularly when the signal constellation contains many points.

Key Words: Carrier Recovery, QAM Receiver, Random Walk Filter, Synchronizer, Communication system, Phase lock loop, Closed loop system

1 INTRODUCTION

A carrier recovery system is a circuit used to estimate and compensate for frequency and phase differences between a received signal's carrier wave and the receiver's local oscillator for the purpose of coherent demodulation. In the transmitter of a communications carrier system, a carrier wave is modulated by a baseband signal. At the receiver the baseband information is extracted from the incoming modulated waveform. In an ideal communications system the carrier frequency oscillators of the transmitter and receiver would be perfectly matched in frequency and phase thereby permitting perfect coherent demodulation of the modulated baseband signal. However, transmitters and receivers rarely share the same carrier frequency oscillator. Communications receiver systems are usually independent of transmitting systems and contain their own oscillators with frequency and phase offsets and instabilities. Doppler shift may also contribute to frequency differences in mobile radio frequency communications systems. All these frequency and phase variations must be estimated using information in the received signal to reproduce or recover the carrier signal at the receiver and permit coherent demodulation. For a quiet carrier or a signal containing a dominant carrier spectral line, carrier recovery can be accomplished with a simple band-pass filter at the carrier frequency and/or with a phase-locked loop [1].

However, many modulation schemes make this simple approach impractical because most signal power is devoted to modulation, where the information is present and not to the carrier frequency. Reducing the carrier power results in greater transmitter efficiency. Different methods must be employed to recover the carrier in these conditions. Blind carrier recovery methods do not rely on any knowledge of the modulation symbols. They are typically used for simple carrier recovery schemes or as the initial method of coarse carrier frequency recovery [2]. Closed-loop non-data-aided systems are frequently maximum likelihood frequency error detectors [3]. In this method of non-data-aided carrier recovery a non-linear operation is applied to the modulated signal to create harmonics of the carrier frequency with the modulation removed. The carrier harmonic is then band-pass filtered and frequency divided to recover the carrier frequency. Multiply-filter-divide is an example of open-loop carrier recovery, which is favored in burst transactions since the acquisition time is typically shorter than for close-loop synchronizers. If the phase-offset/delay of the multiply-filter-divide system is known, it can be compensated for to recover the correct phase. In practice, applying this phase compensation Carrier frequency and phase recovery as well as demodulation can be accomplished using a Costas loop of the appropriate order [4]. A Costas loop is a cousin of the PLL that uses coherent quadrature signals to measure phase error. This phase error is used to discipline the loop's oscillator. The quadrature signals, once properly aligned/recovered, also successfully demodulate the signal. Costas loop carrier recovery may be used for any M-ary PSK modulation scheme [4]. One of the Costas Loop's inherent shortcomings is a 360/M degree phase ambiguity present on the demodulated output is difficult [3]. At the start of the carrier recovery process it is possible to achieve symbol synchronization prior to full carrier recovery because symbol timing can be determined without knowledge of the carrier phase or the carrier's minor frequency variation/offset[5]. In decision directed carrier recovery the output of a symbol decoder is fed to a comparison circuit and the phase difference/error between the decoded symbol and the received signal is used to discipline the local oscillator. Decision directed methods are suited to synchronizing frequency differences that are less than the symbol rate because comparisons are performed on symbols at, or near, the symbol rate. Other frequency

recovery methods may be necessary to achieve initial frequency acquisition.

A common form of decision directed carrier recovery begins with quadrature phase correlators producing in-phase and quadrature signals representing a symbol coordinate in the complex plane. This point should correspond to a location in the modulation constellation diagram. The phase error between the received value and nearest/decoded symbol is calculated using arc tangent (or an approximation). However, arc tangent, can only compute a phase correction between 0 and π / 2. Most QAM constellations also have π / 2 phase symmetry. Both of these shortcomings came be overcome by the use of differential coding [2].

2 QAM RECEIVER

The block diagram of the QAM receiver is as shown in figure 1. The top half of the figure is called as receiver front end. The input signal $r_0(t)$ represents the signal at the receiver input which is the transmitted QAM signal distorted by the non-ideal frequency response of the channel and additive noise. This signal is passed through the Receive Filter which is a bandpass filter that passes the QAM signal and eliminates out-of-band noise. The Receive Filter can also be used in combination with the transmitter filters to perform the spectral shaping required for no intersymbol interference with a perfect channel. In transmission through a communications channel like a voiceband telephone circuit, the signal is often significantly attenuated. Therefore, the output of the Receive Filter is scaled by the automatic gain control (AGC) to increase its amplitude to a level that fully loads the ADC. This scaled signal $r(t)$is sampled at a rate f_0=$1/T_0 = n_0/T$ that is n_o times the symbol rate $f_s = 1/T$ and is at least twice the highest frequency component in the QAM signal to satisfy the sampling theorem. The ADC output samples $r(nT_0)$ are used to adjust the AGC gain. These samples are also used by the Carrier Detect block to determine when a QAM signal is actually present at the receiver input and not just channel noise. Many of the receiver functions are not started until the input signal is detected. The proper sampling times for ADC are determined from the ADC output samples by the Symbol Clock Recovery subsystem. The frequency and phase of the symbol clock must be tracked by this subsystem. The ADC block could be a converter with hardware capability for shifting the sampling phase, or an ADC with a fixed sampling phase combined with a variable phase interpolator implemented by the DSP. Finally the receiver front end forms the pre-envelope $r + nT_0$ of the received signal. The subsystem that forms the pre-envelope is often called a phase splitter.

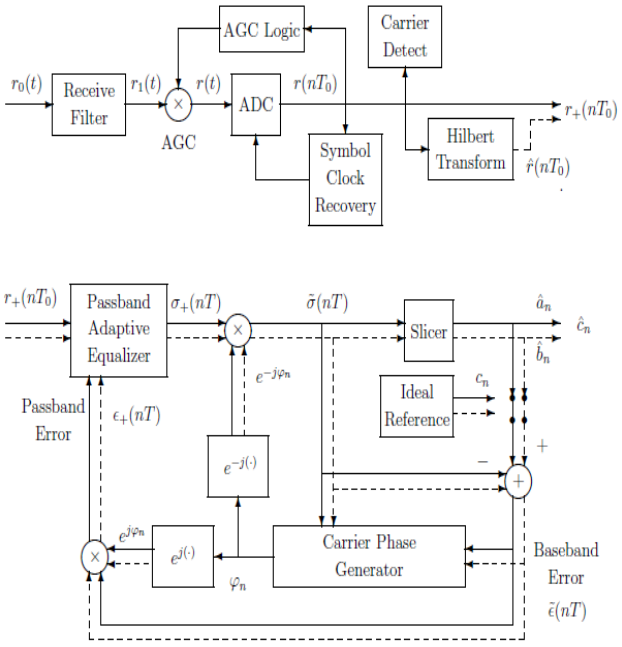

Fig.1 Block Diagram of a QAM Receiver

A real channel does not have a flat amplitude response and constant envelope delay and this causes intersymbol interference in the received signal. The Passband Adaptive Equalizer compensates for the channel response to minimize intersymbol interference. An adaptive filter is used because the exact frequency response of the channel is rarely known. For example, in the switched telephone network, a different channel can be selected each time a new call is made. The equalizer is an adaptive FIR filter that operates on samples spaced by T / n_1 and generates output samples spaced by the symbol period T. The constant n_0 which determines the input sampling period T0 = T / n0 must be divisible by n_1. This is called a fractionally spaced equalizer. We will use $n_1 = 2$. The equalizer input sequence $r + (nT_1 / T)$ is obtained by skip sampling the sequence $r + (nT_0) = r + (nT / n_0)$ Actually, this sampling rate reduction can be performed by having the FIR Hilbert transform filter operate on the T0 spaced samples $r(nT_0)$and computing its output only at the desired times nT / n_1. The equalizer output $\sigma + nT$ is multiplied by the locally generated carrier reference $e^{-j\emptyset_n}$ to demodulate it to the baseband signal $\sigma(nT)$. If all the system components were perfect, the baseband signal samples would be ideal constellation points. In practice, they deviate from the ideal points due to noise and intersymbol interference. The Slicer quantizes the baseband samples to the nearest ideal constellation points which are used as the receiver's estimates of the transmitted symbols. When the adaptive equalizer is working well and the carrier reference is good, the quantized output symbols will be the same as the transmitted symbols with high probability. The local carrier reference can be synchronized with the received signal's

carrier by using the transmitted constellation sequence and the baseband error $c_n - \sigma(nT)$ between the transmitted sequence and baseband equalizer output. The Carrier Phase Generator block performs this function. During an initial training period, the Ideal Reference generator is used to create a local replica of the known transmitted training sequence. After that, the outputs of the slicer are used as good estimates of the transmitted symbols. This is called decision directed operation. The equalizer coefficients are adjusted by a least mean-square error algorithm which uses the passband error. A significant portion of the initial training sequence is used to adjust the adaptive equalizer. The carrier recovery loop typically converges much faster than the equalizer. The receiver described is one of several approaches. Some modem designers prefer to remove the Hilbert Transform block and force an adaptive equalizer that operates on the real samples $r(nT_0)$ with two sets of real coefficients to perform both the equalization and phase splitting simultaneously.

3 RECEIVER FRONT-END SUBSYSTEMS

In this section, more details about how to implement most of the receiver front-end subsystems are presented.

3.1 Automatic Gain Control

The purpose of the automatic gain control (AGC) is to scale the analog input voltage to a level that almost fully loads the ADC but avoids clipping. Various combinations of strategies can be used. For example, the peak magnitude of the digitized samples can be monitored for a fixed time period and the analog gain can be adjusted to load the ADC converter to a desired level with some margin against clipping. This peak detection method can be combined with a scaling function that adjusts the average power of the sequence of samples to a desired level.

3.2 The Carrier Detect Subsystem

The purpose of the Carrier Detect subsystem is to determine when a QAM modem signal is present at the receiver input and not just channel noise. Generally it is considered that a carrier has been detected when it is decided that a modem signal is being received. When no QAM signal is present, the receiver is kept in a default state waiting for a known training sequence to begin. When no carrier is detected, some of the things the receiver does are: (1) set the AGC to a higher gain, (2) set the EIA RS232 output levels for clear-to-send (CTS) and carrier detect (CD) to the off state (−12 v), (3) clamp the output data to steady marks (logical 1 or −12 v), (4) keep the equalizer taps cleared to zero and set the equalizer adaptation speed control to a fast value, (5) keep the frequency offset variable cleared in the carrier tracking loop, and (6) put the symbol clock tracking loop in a fast mode. One approach to carrier detection is to form a running estimate of the received signal power. This power estimate can be formed by passing the squared ADC output samples through a first-order recursive low pass filter with the transfer function:

$$H(z) = \frac{1-c}{1-cz^{-1}} \quad (1)$$

The constant c is a number slightly less than 1. The closer c is to 1, the narrower band the lowpass filter is, but the slower it is to reach steady state. The numerator 1 − c was chosen to make the gain 1 at zero frequency. The resulting equation for the power estimate is

$$p(n) = (1-c)r^2(nT_0) + cp(n-1) \quad (2)$$

This is sometimes called exponential averaging. When the power estimate exceeds a predetermined threshold for a period of time, a received modem signal is declared to be present. Once a carrier is detected, the threshold should be reduced by 5 dB. Another function of the Carrier Detect box is to detect when the received modem signal stops. This is called loss of carrier. Loss of carrier is declared when $p(n)$ falls below the reduced threshold for a period of time. The threshold hysteresis is used to avoid false detection of carrier loss caused by the random fluctuations of $p(n)$. According to recommendation V.22 bis, the carrier detect (CD) RS-232C connector signal should be turned off 40 to 65 ms after the power level of the received input signal falls below the lower threshold. It should be turned off in 10 to 24 ms for the V.22 modem.

3.3 Symbol Clock Recovery

At the receiver, the transmitter's symbol clock frequency is known quite accurately, but not perfectly. The clock phase is completely unknown and can be modeled as a random variable uniformly distributed over one symbol period. However, any error in the clock frequency will cause the equalizer timing reference to drift towards one end of its delay line and fall off that end at which point the receiver crashes. Therefore, the clock frequency must be tracked very closely. An idealized block diagram for this scheme is shown in Figure 2. The ADC samples the analog input signal $r(t)$ at the frequency $f_0 = 1/T_0 = n_0 f_s$ where $f_s = 1/T$ is the symbol rate and n_0 is chosen so the sampling frequency satisfies the Nyquist criterion. Thus, the sampling instants are $nT_0 + \tau$ where τ represents the clock phase. This phase varies with time because of clock frequency offsets between the transmitter and receiver and adjustments made by the receiver's tracking algorithm. The goal of the tracking loop is to adjust the sampling frequency so that it is n_0 times the true symbol frequency and then drive τ to zero.

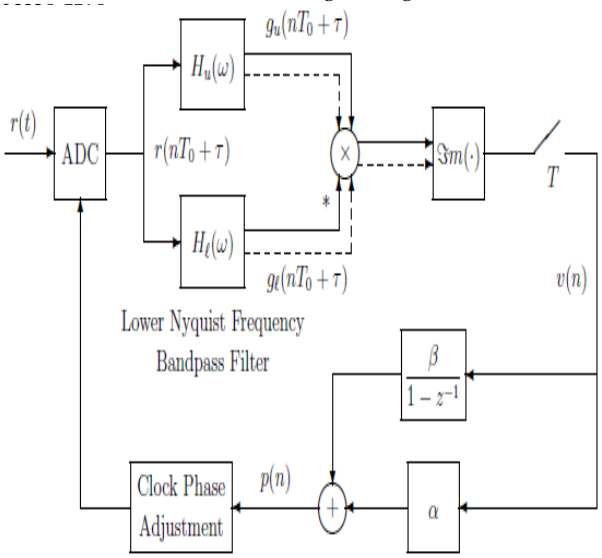

Fig.2 General Block Diagram of Symbol clock Tracking Loop

The samples are applied to two bandpass filters operating at the sampling rate of $f_0 = n_0 f_s$. One filter is tuned to the upper Nyquist frequency ω_u=ω_c+0.5f_s and the other to the lower Nyquist frequency$\omega_l = \omega_c - 0.5f_s$. Let the responses of these filters over the Nyquist band $|\omega| < 0.5f_0$ be

$$H_u(w) = \begin{cases} 2 \; for \left| w - w_u \right| < B/2 \\ 0 elsewhere \end{cases} \quad (3)$$

and

$$H_l(w) = \begin{cases} 2 \; for \left| w - w_l \right| < B/2 \\ 0 \text{ elsewhere} \end{cases}$$

$$\text{T0} = \text{T} / \text{n0}$$

$$\text{n}_1 = 2 \quad (4)$$

$$\text{r} + (\text{nT}_0) = \text{r} + (\text{nT} / \text{n}_0).$$

$$\text{nT} / \text{n}_1$$

The bandwidth B/2 should be reasonably should be reasonably small, for example, 100 Hz for a f_s=2400 baud modem. Notice that these filters only pass positive frequency components and have complex impulse responses.

The complex output of the upper Nyquist frequency bandpass filter is multiplied by the complex conjugate of the output of the lower Nyquist frequency bandpass filter. The imaginary part of this product is sampled at the symbol rate$f_s = 1/T$. It will be shown in an example below that the resulting sequence $v(n)$gives an estimate of the timing phase error. Each symbol period, the clock phase is advanced or retarded by an amount α times the phase error plus an amount β times the accumulated phase error. That is, the phase advancement increment is

$$p(n) = \alpha v(n) + \beta \gamma(n) \quad (4)$$

Where

$$\gamma(n) = v(n) + \gamma(n-1) \quad (5)$$

The accumulator is included to make the timing recovery loop track frequency offsets. Using the correct polarity for the clock phase adjustment is critically important. Using the wrong phase, results in an unstable loop. When $p(n)$ is positive, the sampling instants are occurring too late. In this case, the time to the next sample should be reduced by $p(n)$. Similarly, when $p(n$ is negative, the sampling instants are occurring too early and the time to the next sample should be increased by $|p(n)| = -p(n)$. To see how this system generates symbol clock control information, suppose the transmitted symbol sequence is

$$c_n = (-1)^n = \cos n\pi = \cos 0.5\omega_s nT \quad (6)$$

If the baseband transmit filter has raised cosine spectral shaping so that it has no intersymbol interference, the baseband complex envelope of the transmitted signal is

$$s(t) = \cos 0.5\omega_s t$$

Notice that the correct sampling instants are at times nT where the pre-envelope has the values (−1) n. The transmitter output has the pre-envelope

$$S_+(t) = \cos 0.5\omega_s t e^{j(\omega_c + 0.5\omega_s)t} + 0.5e^{j(\omega_c - 0.5\omega_s)t} \quad (7)$$

Thus, the transmitted signal is the sum of sinusoids at the upper and lower Nyquist frequencies. The output of the upper Nyquist frequency bandpass filter is

$$\text{g\_u (nT\_0+}\tau\text{)} = e^{j(\omega_c + 0.5\omega_s)(nT_0 + \tau)} \quad (8)$$

and the output of the lower Nyquist frequency bandpass filter is

$$g_l(nT_0 + \tau) = e^{j(\omega_c - 0.5\omega_s)(nT_0 + \tau)} \quad (9)$$

The multiplier output is

$$q(nT_0 + \tau) = g_u(nT_0 + \tau) g_l(nT_0 + \tau) = e^{j\omega_s\left(\frac{nT_0}{n_0} + \tau\right)} \quad (10)$$

Replacing n by $mn_0$to evaluate this signal once per symbol and taking the imaginary part

Gives $v(n) = \zeta mq(nT + \tau) = \sin\omega_s \tau$ (11)

When$|\omega_s\tau| < \pi$, $v(n)$has the same polarity as the sampling phase error τ . Also, when

$|\omega_s\tau| \ll 1$, $\sin\omega_s\tau$ is closely approximated by the linear function $\omega_s\tau$.

The block diagram for a practical realization of the symbol clock tracking loop is shown in Figure 14.3. The upper Nyquist frequency bandpass filter is approximated by a filter with a single complex pole at $z = ve^{j\omega_u T_0}$. Its transfer function is

$$H_u = \frac{1}{1 - ve^{j\omega_u T_0} z^{-1}} = \frac{1 - ve^{-j\omega_u T_0} z^{-1}}{(1 - ve^{j\omega_u T_0} z^{-1})(1 - ve^{-j\omega_u T_0} z^{-1})}$$

$$= \frac{1 - z^{-1} v\cos\omega_u T_0}{1 - z^{-1} 2v\cos\omega_u T_0 + v^2 z^{-2}} + j\frac{z^{-1} v\sin\omega_u T_0}{1 - z^{-1} 2v\cos\omega_u T_0 + v^2 z^{-2}} \quad (12)$$

The amplitude response of this filter has a peak value of 1/1-v at the upper Nyquist frequencyω_u. The bandwidth of the filter is determined by the parameter v which should

be in the range [0, 1]. The closer v is to 1, the narrower the bandwidth. The method used to compute the complex output from the real $\rho(n) = r(nT_0 + \tau)$ (13).

The first step is to compute the intermediate real variable

$$\eta(n) = \rho(n) + 2v\cos\omega_u T_0)\eta(n-1) - v^2\eta(n-2) \quad (14)$$

This recursion must be computed at the fast input sampling rate$f_0 = n_0 f_s$. The real and Imaginary parts of the output are computed as

$$\Re e\{g_u(nT_0 + \tau)\} = \eta(n) - v\cos(\omega_u T_0)\eta(n-1) \quad (15)$$

and

$$\zeta m\{g_u(nT_0 + \tau)\} = v\sin(\omega_u T_0)\eta(n-1) \quad (16)$$

The real and imaginary parts only have to be computed at the symbol rate f_s . The lower Nyquist bandpass filter is implemented in a similar manner by simply replacing u by l in the previous equations.

The imaginary part of the product $g_u(nT_0 + \tau)g_l(nT_0 + \tau)$ is computed once per symbol as shown in Figure 3 to form the timing error signal $v(n)$ .This signal has significant variability when random data is transmitted. The variability increases as the number of points in the constellation increases. The philosophy for adjusting the symbol clock sampling phase is similar to the approach used in the phase-locked loops in previous experiments. The variability in $v(n)$ is lowpass filtered by incrementing the clock phase by a small fraction α of $v(n)$ each symbol. In addition, $v(n)$ is accumulated to detect any DC component caused by a clock frequency offset, and a small fraction β of the accumulation is added to the clock phase increment. For good transient response, β should be a factor of 50 to 100 times less than α . The tracking loop becomes more narrow band as α is decreased.

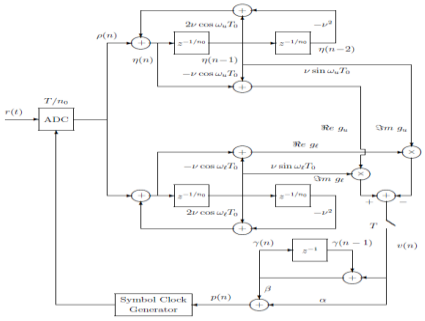

Fig.3 Practical Realization of symbol clock Tracking Loop

3.4 An Additional Suggestion for Rapid Symbol Clock Acquisition

The bandwidth of the clock tracking loop should be very small to make the clock jitter negligible. It also must be small to make the loop stable in light of significant delays in the loop from the time the phase updates are made to the time they propagate through the system components to the phase error measurements. This means the loop transient response will be very slow. If the local symbol clock is far off in phase from the clock in the received signal, the loop will take a long time to slew around to the correct position. The worst case is when the clocks are 180 degrees out of phase. During the initial training sequence for many modems a dotting sequence like the S1 sequence is transmitted for a short period of time. The dotting sequence has strong components at the carrier frequency plus or minus half the symbol rate and the output of the Godard clock tone generation system is a strong tone at the symbol rate. This tone can be used to rapidly lock on to the symbol clock. The clock tracking loop updating can be turned off and the symbol rate samples of the complex multiplier output,

$$q(nT_0+\tau)=g_u(nT_0+\tau)g_l(nT_0+\tau) \quad (17)$$

can be observed for a period of time during the dotting sequence and their phase measured. Suppose the measured phase is θ_n. Then $q(n)$ can be multiplied by $\exp(-j\theta_q)$ to form the complex signal,

$$q(nT+\tau)=q(nT+\tau)e^{-j\theta_q} \quad (18)$$

this has an angle of zero. Geometrically, this is equivalent to rotating the complex clock tone sample to point in the positive real direction. The imaginary part of $q(nT+\tau)$ will then be zero. Then the loop updating can be turned on with $\zeta mq(nT+\tau)$ used as the signal $v(n)$ that specifies the clock phase update increments. In effect, this fools the loop into thinking it is initially at the correct phase and it does not have to move from this position. The fractionally spaced equalizer will compensate for any fixed phase offset.

3.5 Random Walk Filter in the Symbol Clock Tracking Loop

In practice, it has been found that the signal $p(n)$ shown in Figure 3 must be additionally filtered to reduce symbol clock jitter, particularly when the signal constellation contains many points. A technique called a random walk filter has been found to work well and is shown in Figure 4. First, the output of the Godard band edge filter cross-correlator is hard limited to form the signal The hard limiting provides a simple AGC action that keeps the loop gain constant independent of the input signal level. This signal is then passed through the same kind of second-order loop filter as shown in Figure.3 resulting in the signal $p(n)$.

$$v(n)=sign v(n)=\begin{cases}1 & for\ v(n)>0\\ 0 & for\ v(n)=0\\ -1 & for\ v(n)<0\end{cases} \quad (19)$$

The output of the second-order loop filter is then applied to the random walk filter. The random walk filter is basically an accumulator that gets reset when its output exceeds a positive or negative threshold. The random walk filter accumulator output is

$$y(n)=x(n)+p(n)$$

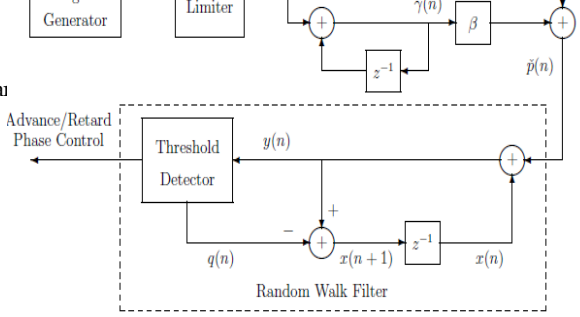

Fig.4 Including a Random Walk Filter in the Clock Tracking Loop

where

$$x(n+1)=y(n)-q(n)=x(n)+p(n)-q(n) \quad (20)$$

The signal $q(n)$ is generated by the Threshold Detector and is zero most of the time. When the accumulator output $y(n)$ exceeds the thresholds of L or $-L$, the accumulator value is reset and the sampling phase of the ADC or variable phase interpolator is advanced or retarded. As long as the accumulator output remains between the thresholds, the sampling phase is not changed. This significantly reduces clock jitter. The exact rules describing the Threshold Detector and accumulator are:

$$q(n)=\begin{cases}0 & for\ |y(n)|<L\\ L & for\ |y(n)|\geq L\\ -L & for\ |y(n)|\leq -L\end{cases} \quad (21)$$

and

$$x(n+1)=\begin{cases}y(n) & for\ |y(n)|<L\\ y(n)-L & for\ y(n)\geq L\\ y(n)+L & for\ y(n)\leq -L\end{cases} \quad (22)$$

When $y(n)$ exceeds the positive threshold L, this indicates that the sampling phase is too late, so the phase must be advanced. When $y(n)$ is algebraically less that the negative threshold, −L, the phase must be retarded. The phase is not changed while $y(n)$ remains between the thresholds.

4 CONCLUSION

This paper presents detailed analytical investigations on the carrier recovery circuit for a 16 QAM receiver used in software defined radio. These investigations will lead to the design of a carrier recovery circuit, which can be implemented efficiently on a field programmable gate array.

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- *Mansi Kapahi is currently pursuing masters degree program in electronics & communication engineering in Punjabi University, India, PH-9815852434. E-mail: mansi.kapahi88@gmail.com*
- *Amandeep Singh Sappal is currently serving as Asst prof in Punjabi University, India,. E-mail: sappal73as@pbi.ac.in*